REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated June 3, 2005. Appreciation is expressed for the allowance of claims 25, 27, 46 and 47.

By the present amendment, Appendix B is provided which includes a marked-up copy of the original Specification, with appropriate underlinings for the added text being provided. Based on this, entry of the Substitute Specification filed on October 27, 2004 is respectfully requested. More specifically, on page 2 of the Office Action, it was indicated that the Substitute Specification filed on October 27, 2004 had not been entered because the text of the added subject matter had not been shown with underlinings in the marked copy. Accordingly, the attached marked copy of the original Specification provides the required underlining.

Also by the present amendment, a replacement sheet of drawings has been provided for Fig. 11 which correctly changes the numeral 24 to the numeral 23. Accordingly, removal of the objection to the drawings set forth on page 2 of the Office Action is respectfully requested.

Also by the present Amendment, the Specification has been amended to provide reference to numerals 22 and 23. Accordingly, removal of the objections to the drawings set forth on page 3 of the Office Action is also respectfully requested.

In addition, claim 32 has been amended to depend on claim 14, rather than claim 31. As such, claim 32 now serves to further limit the subject matter of a previous claim

(that is, claim 14), and, accordingly, removal of the objection regarding claim 32 is respectfully requested.

Reconsideration and removal of the objection to the drawings set forth and beginning with the last two lines on page 3 of the Office Action and continuing through line 8 on page 4 of the Office Action is also respectfully requested. This objection pertains to the language of claim 24. Applicants respectfully submit that the arrangement defined in claim 24 is clearly shown in the present drawings, specifically, in Figs. 2(a)-(c). More specifically, comparing claim 24 with the various drawings of Fig. 2, it is noted that the first direction corresponds to the X direction shown in Fig. 2 while the second direction corresponds to the Y direction. Solely for purposes of example, it is noted that the claimed emitter or source electrodes can be read on the electrodes identified by the numeral 7 in Fig. 2(c). The claimed via holes can be read on the via holes 5 shown in Fig. 2(a)-(c). As shown in Fig. 2(a) and 2(c), the emitter electrodes are arranged in a row extending in the first X direction on a semiconductor substrate 1. The via holes are arranged in a second direction Y, orthogonal to the first direction, as shown in Figs. 2(b) and 2(c). Accordingly, it is respectfully submitted that the present drawings already provide clear support for the features of claim 24, and removal of the objection set forth on the paragraph bridging pages 3 and 4 is respectfully requested.

Similarly, reconsideration and removal of the 35 USC §101 and 35 USC §112, second paragraph, rejection of claims 21, 22 and 39-42 is also respectfully requested. These rejections are based on an argument in the Office Action that they improperly mix device and process classes of invention. In response to this, applicants have amended claims 21 and 22 to further define, within the "wherein clause" that "the through holes

are distributed in the multilayer wiring board so that," prior to the previously existing language concerning the distribution of heat. As such, it is respectfully submitted that these amendments to claims 21 and 22 clearly set forth that the claimed distribution of heat coinciding with the distribution of through holes results from a structural feature of the distribution of through holes itself. This is clearly a device limitation. Therefore, it is respectfully submitted that the independent claims 21 and 22 do not improperly mix device and process statutory classes of invention, but are, instead, proper device claims. Therefore, reconsideration and removal of the 35 USC §102 and 112, second paragraph, rejections of the independent claims 21 and 22, and their dependent claims 39-42, is respectfully requested.

Reconsideration and removal of the rejection of claims 14-20, 23, 26, 28-38, 43-45, 48 and 49 as being anticipated by applicants' admitted prior art is also respectfully requested. With regard to this, it is noted that the specification refers to Figs. 3 and 4 as representing a conventional prior art arrangement. As such, it is applicants understanding that the Examiner's reference to "admitted prior art" is correctly limited to the disclosure concerning Fig. 3 and 4, both of which are identified as either "a Prior Art Semiconductor Substrate and a Multilayer Wiring board" (Fig. 3) or "a Prior Semiconductor Substrate." (Fig. 4). However, as clearly set forth in paragraph [0056] of the Substitute Specification:

> " As mentioned above, Figs. 3 and 4 are views showing an exemplary arrangement of a conventional semiconductor substrate 1 and a multilayer wiring board 3, in which the positional relationship between the thermal vias 4 and via holes 5 is not prescribed. Therefore, there is caused a problem that, as shown in the plan view in Fig. 4, the via holes 5 and thermal vias 4 become out of position relative to each other. Accordingly, even though the multilayer wiring board 3 has thermal resistance as an element equivalent to that of the embodiment of the

> present invention shown in Figs. 1 and 2, thermal resistance of the entire structure is increased in terms of radiation paths in the planar direction."

This lack of alignment between the via holes 5 of the semiconductor device and the thermal vias 4 of the multilayer wiring board can clearly be appreciated by comparing the prior art Fig. 4 (where the vias 5 are not aligned with the thermal vias 4) and Fig. 2 (where the via holes 5 are clearly aligned with the thermal vias 4).

As such, it is respectfully submitted that claims 14-20, 23, 26, 28-38, 43-45, 48 and 49 all clearly define structural arrangements which are neither taught nor suggested by the admitted prior art of Figs. 3 and 4. Taking claim 14 as an example, an arrangement is defined:

> "Wherein the through holes in the semiconductor substrate are located relative to the through holes in the multilayer wiring board so that entire areas, which the through holes in a semiconductor substrate occupy, in a plane orthogonal to the thickness-wire direction of the multilayer wiring board and of the semiconductor substrate are included in areas which the through holes in the multilayer wiring board occupy."

This can clearly be read on Fig. 2(c), where the via holes 5 are aligned with the thermal vias 4. However, this limitation clearly cannot be read on the prior art arrangement shown in Fig. 4 where the via holes 5 are clearly not included in the areas in which the through holes 4 in the multilayer wiring board occupy. Therefore, it is respectfully submitted that the admitted prior art of Figs. 3 and 4 clearly does not anticipate the recitations found in claims 14-20, 23, 26, 28-38, 43-45, 48 and 49 regarding the relationship between the via holes 5 of the semiconductor device and the thermal vias 4 of the multilayer wiring board. Therefore, reconsideration and removal of the 35 USC §102(a) rejection set forth in the Office Action regarding these claims is respectfully requested.

Reconsideration and removal of the 35 USC §103(a) rejection of claim 24 as being unpatentable over applicants admitted prior art is also respectfully requested. In the Office Action, it is recognized that the admitted prior art "does not appear to explicitly admit as prior art that the rows comprise emitter electrodes or source electrodes, and the via holes are arranged in parallel in a second direction orthogonal to the first direction. " As discussed above, the relative arrangement of the rows of emitter or source electrodes in the first direction and the via holes in an orthogonal second direction can be seen, for example, in Figs. 2(a)-2(c). Notwithstanding this recognition of the distinction of claim 24 over the admitted prior art, page 14 of the Office Action goes on to state that it would be "an obvious matter of design choice ... to arrange the rows of the admitted prior art as claimed because applicant is not disclosed that, in view of the applied prior art, the arrangement is for any purpose, produces an unexpected result, or is otherwise critical, and it appears *prima facie* that the process would possess utility using another arrangement."

As a result, no documentary evidence is provided to establish the motivation to modify the admitted prior art.

With regard to this, attention is respectfully directed to MPEP 2144.03 which pertains to Reliance on Common Knowledge in the Art or "Well Known" Prior Art." As stated in this section of the Manual:

> "It is never appropriate to rely solely on "common knowledge" in the art <u>without evidentiary support in the record, as the principle evidence upon which a rejection was based."</u>

It is respectfully submitted that, in the present instance, the rejection of claim 24 is based solely upon "common knowledge." MPEP 2144.03 also points out that:

> Official notice unsupported by documentary evidence should only be taken by the Examiner where the facts asserted to be well known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well known."

In the present instance, there has been no demonstration whatsoever that the modifications necessary to the admitted prior art to arrive at the invention defined by claim 24 are "capable of instant and unquestionable demonstration as being well known." Instead, the Office Action simply states that the applicants have failed to show any unexpected result or any criticality to the applicants different claim structure. With regard to this, the specification does, in fact, clearly define that the object of the invention is to provide a multilayer wiring board "in which thermal resistance of radiation paths is reduced to provide an improvement in radiation effect." The structure defined by claim 24 is directed to such an object, and differs from the arrangement of the admitted prior art of Figs. 3 and 4. This difference in structure is apparently recognized in the Office Action. Accordingly, in light of the failure of the Office Action to provide any documentary evidence showing that it would be obvious to modify the arrangement of Fig. 3 and 4 to arrive at the different structure of claim 24, reconsideration and removal of the 35 USC §103 rejection of claim 24 is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this

paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 500.40530X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Gregory E. Montone
Reg. No. 28,141

GEM/dks
N:\500\40530X00\AMD\CJ8599.DOC

1300 North Seventeenth Street, Suite 1800
Arlington, Virginia 22209
Telephone: (703) 312-6600
Facsimile: (703) 312-6666

AMENDMENTS TO THE DRAWINGS

The attached sheet of drawing includes changes to Fig. 11. This sheet, which includes Fig. 11, replaces the original sheet including Fig. 11. In Fig. 11, the numeral 24 has been correctly changed to numeral 23.

MULTILAYER WIRING BOARD AND SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device such as a multifinger type device used in high-frequency power amplifiers for portable communication terminal.

Power enabling communication from a position distant from a communication relay point is required of portable communication terminals such as portable telephones, and thus high-frequency power amplifiers in portable communication terminals have been increased in capacity.

As a measure for increasing high-frequency power amplifiers in capacity, it is possible to provide an increase in current for high output by modularizing and arranging many bipolar transistors (hereafter, referred to as transistors) in parallel at predetermined spacing.

However, if transistors are arranged in parallel at predetermined spacing, centrally positioned transistors are thermally affected by adjacent transistors to become highest in thermal resistance (hereinafter referred to as calorific value).

In this manner, when transistors having high calorific values are present among transistors arranged in parallel, current flows through transistors of high

calorific values in a concentrated manner, and hence, the transistors possibly suffer thermorunaway ~~to be broken~~ which can lead to a breakdown of the transistors.

Therefore, it is conventional that transistors in such arrangements are varied in size according to calorific values thereof. An example of such a ~~In addition, this kind of~~ conventional technique is disclosed in, for example, Japanese Patent Unexamined Publication Nos. 2-219298 and 5-152340.

In recent years, it has been increasingly demanded to make portable communication terminals small in size, lightweight, and low in cost, as well as to increase their power amplifiers in power, as mentioned above. As matters stand, it is naturally inevitable ~~to~~ that the ~~miniaturize~~ power amplifiers must be miniaturized. ~~Thereupon~~ As such, when transistors themselves are made small in order to miniaturize a power amplifier, it is found that a heating temperature of transistors is undesirably high for disposed on ends of a row of the transistors arranged in parallel ~~is high~~. The reason for this is believed to be that, while heat generated in centrally positioned transistors is transferred and diffused to adjacent transistors, heat transfer is small in endwise positioned at the ends of the group of transistors. This positioned transistors to cause an increase in calorific value for such end transistors since there are transistors only on one side of the end transistors to which heat should can be diffused.

In the case where as a measure is provided for cooling such heat, thermal vias are can be formed in a wiring board as

disclosed in Japanese Patent Unexamined Publication No. 2-219298, with such an arrangement, it is possible that heat distribution inside a semiconductor substrate makes it impossible to ignore a portion of the heat which flows in a direction (hereinafter, referred to as "planar direction") orthogonal to a thickness-wise direction of the semiconductor substrate, in addition to one-dimensional flow of heat in the thermal vias, in the event of insufficient diffusion of heat in the semiconductor substrate. That is, when heating areas in the semiconductor substrate are distant from positions of the thermal vias in the planar direction in a wiring board, thermal resistance correspondingly increases.

Also, when radiation paths in a wiring board which mounts a semiconductor substrate are not suitable, as in the case where via holes and PHS are used, as disclosed in Japanese Patent Unexamined Publication No. 5-152340, it is difficult to reduce thermal resistance. In particular, there is a need of making PHS, which an expensive material such as gold plating is used to form, as thin as possible in thickness from a viewpoint of cost reduction. However, when PHS is made thin, diffusion of heat in a PHS layer becomes extremely insufficient in a planar direction, and while thermal diffusion remains insufficient, heat is conducted to a multilayer wiring board via a brazing material. Therefore, when via holes and thermal vias are positionally distant from each other, thermal resistance of the

entire wiring board cannot be reduced from a semiconductor device with the result that the via holes and thermal vias cannot serve as radiation paths.

Further, in the case where a semiconductor substrate having a small thermal conductivity, like a GaAs substrate ~~is used~~, and in the case where an insulating film adapted to function as a thermally insulating material is present between a device circuit surface and a substrate mother material like a SOI (silicon on insulator) substrate, there is the possibility that radiation electrodes provided on that surface of the semiconductor substrate, on which a circuit is formed, serve inadequately due to the fact that thermal resistance of paths, along which heat is discharged to the semiconductor substrate and the wiring board from heating areas such as emitter base junctions through wiring and radiation electrodes, becomes larger than that of paths, along which heat is discharged directly to a back surface of the semiconductor substrate from the heating areas, because thermal resistance is increased when heat passes through the semiconductor substrate. In the well-known technique disclosed in Japanese Patent Unexamined Publication No. 8-227896, radiation electrodes are simply formed on a semiconductor substrate with a diffusion layer for contact therebetween, and ~~so~~ such technique cannot be said to be sufficiently effective from a viewpoint of heat radiation in a thickness-wise

direction of a semiconductor substrate, a wiring board, or a semiconductor substrate.

In this manner, any conventional technique cannot provide ideal heat radiation.

An object of the present invention is to provide a multilayer wiring board, in which thermal resistance of radiation paths is reduced to provide an improvement in radiation effect.

SUMMARY OF THE INVENTION

The above object is attained by a multilayer wiring board having through-holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has through-holes in a thickness-wise direction thereof, and entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which the through holes in the multilayer wiring board occupy.

Also, the above object is attained by a multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has through-holes in a thickness-wise direction thereof, and entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal

to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate partly overlap areas which the through holes in the multilayer wiring board occupy.

Also, the above object is attained by a multilayer wiring board having a through hole or holes in a thickness-wise direction, wherein respective heating areas inside a semiconductor substrate mounted on the multilayer wiring board are included in areas, which the single or plural through holes in the multilayer wiring board occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate.

Also, the above object is attained by a multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has through holes in a thickness-wise direction thereof, and in this arrangement, heat flow one-dimensionally through the through holes in the semiconductor substrate and the through holes in the multilayer wiring board in the thickness-wise direction when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board.

Also, the above object is attained by an

arrangement in which conductive layers are formed on side surfaces of the through holes, or interiors of the through holes ~~comprise~~ are formed of a conductive material.

Also, the above object is attained by an arrangement in which a semiconductor element is mounted, in which conductive layers are formed on side surfaces of the through holes, or in which interiors of the through holes ~~comprise~~ are formed of a conductive material.

Also, the above object is attained by an arrangement in which wirings, which connect heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, ~~and~~ With this arrangement, electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order.

Also, the above object is attained by a multilayer wiring board having through holes in a thickness-wise direction, wherein the distribution density of calorific values in a plane orthogonal to the thickness-wise direction of a semiconductor substrate mounted on the multilayer wiring board substantially coincides with the distribution density in a plane orthogonal to the thickness-wise direction of the through holes.

Also, the above object is attained by a multilayer wiring board having through holes in a thickness-wise direction, wherein the distribution density of calorific values in a plane orthogonal to the thickness-wise direction of a semiconductor substrate mounted on the multilayer wiring board substantially coincides with the distribution density of large and small cross-sectional areas in a plane orthogonal to the thickness-wise direction of the through holes.

Also, the above object is attained by a wiring board, wherein a semiconductor substrate having through holes, which are connected to emitter wirings connected to emitters of heterojunction bipolar transistors and extend through the semiconductor substrate in a thickness-wise direction and which have conductive layers on sides thereof or inside thereof, is mounted on the multilayer wiring board, and the through holes in the semiconductor substrate and the through holes extending through the wiring board in a thickness-wise direction are connected to each other, ~~and wherein~~ In this arrangement, conductive layers are provided on sides of or inside of the through holes in the semiconductor substrate and the wiring board, and areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas, which the through

holes in the multilayer wiring board occupy.

Also, the above object is attained by a multilayer wiring board, wherein emitter fingers of heterojunction bipolar transistors are arranged on a semiconductor substrate, the semiconductor substrate is mounted on a wiring board, which has through holes in a thickness-wise direction, and the through holes in the wiring board have on sides or inside thereof a material of good thermal conductivity, ~~and wherein~~ In this arrangement, areas, which emitter fingers, except these emitter fingers at both ends of the emitter fingers, electrically connected by the same emitter wirings occupy in a plane orthogonal to the thickness-wise direction of the semiconductor substrate and the wiring board, are included in areas which the through holes in the wiring board occupy, ~~but~~ On the other hand, areas, which the fingers at the both ends occupy, are not included therein.

Also, the above object is attained by a semiconductor device including a plurality of finger-like emitter electrodes or source electrodes, and at least one via hole arranged in rows in a first direction on a semiconductor substrate, in which semiconductor device the emitter electrodes or the source electrodes are connected to a conductive layer formed on a back surface opposite to that surface, on which the electrodes are formed, through the via hole, ~~and in which~~ In this arrangement, the semiconductor device rows comprising the emitter electrodes or source electrodes, and the via hole are

arranged in parallel in a second direction orthogonal to the first direction, and the via holes are positionally offset from one another among adjacent rows, or adjacent rows are positionally offset from one another.

Also, the above object is attained by an arrangement, in which the multilayer wiring board has through holes formed on sides thereof or inside thereof with a conductive layer, and areas, which the via hole of the semiconductor device occupies, overlap areas, which the through holes of the multilayer wiring board occupy in a plane orthogonal to the thickness-wise direction.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross sectional view of a multilayer wiring board according to the present invention.

Figs. 2A to 2C are views showing a fundamental embodiment according to the present invention.

Fig. 3 is a cross sectional view showing a prior art semiconductor substrate and a multilayer wiring board in the prior art.

Fig. 4 is a view showing the positional relationship between via holes and thermal vias in a prior semiconductor substrate.

Fig. 5 is a cross sectional view showing an embodiment, in which thermal vias are arranged below heating areas.

Fig. 6 is a cross sectional view showing heat flows in a semiconductor substrate.

Fig. 7 is a cross sectional view showing an embodiment, in which thermal vias are arranged below via holes and heating areas.

Fig. 8 is a cross sectional view showing an embodiment, in which thermal vias are arranged below only central portions of heating areas.

Fig. 9 is a cross sectional view showing an embodiment, in which a circuit surface is formed on an SOI substrate.

Fig. 10 is a cross sectional view showing a typical cross-sectional structure of a prior hetero-junction bipolar transistor.

Fig. 11 is a view showing an arrangement of electrodes and via holes in a prior semiconductor substrate.

Fig. 12 is a view showing an embodiment, in which via holes are positionally offset between adjacent rows.

Fig. 13 is a view showing an embodiment, in which rows of emitters are positionally offset between adjacent rows.

Fig. 14 is a view showing an embodiment, in which rows of emitters are positionally offset between adjacent rows and via holes and thermal vias positionally overlap one another.

DESCRIPTION OF THE EMBODIMENTS

Incidentally, a semiconductor device used in high frequency power amplifiers for pocket communication terminals etc. is constituted conventionally, as shown in Fig. 3, by stacking a multilayer wiring board 3, a brazing material 2, and a semiconductor device 1 in this order from below. In a semiconductor device of such structure, though not shown, a plurality of parts, such as a chip capacitor and a resistor, as well as the above-described semiconductor device 1, are mounted on the wiring substrate 3.

Also, a mother material of the above-described multilayer wiring board 3 is a ceramic-based, a glass-ceramic-based, or a glass-epoxy-based electric insulating material. Generally, there has been caused a problem that, since electric insulating materials also have a low thermal conductivity, they in use while in an original state result in an increase in thermal resistance of an entire device, and even if a back side of the device is kept at temperature below a certain value, a heating area in the semiconductor device extremely rises in temperature to cause thermorunaway of or breakage, in some cases, of the device.

In order to solve the problem, that technique is adopted in which a plurality of pillar-shaped members (hereinafter, referred to as "thermal via") 4 with conductivity and high thermal conductivity are arranged to substantially extend through the multilayer

wiring board 3 in a thickness-wise direction, a semiconductor device 1 is mounted thereon by means of a conductive brazing material 2 such as solder, the thermal vias are connected to a common grounding electrode on a mother board from a back side of the multilayer wiring board 3 and thermal connection is also ensured therebetween to reduce thermal resistance between heating areas in the semiconductor device 1 and the back side of the wiring board 3.

Meanwhile, in order to enhance output and efficiency of the power amplifier, there has been developed a device of the type in which hetero-bipolar transistors (HBTs) are formed on a compound semiconductor substrate such as GaAs or the like. Fig. 10 shows an exemplary cross sectional structure of the device and Fig. 11 shows an exemplary plan in the case where a plurality of comb-type finger electrodes are aligned. Such compound semiconductor substrate suffer from involves a problem that it has they have low thermal conductivity as compared with Si-based substrates, and is insulating are effectively except for portions which are used to form semiconductor devices. Therefore, in the case where a compound semiconductor substrate such as GaAs is used to form a semiconductor device, a technique is adopted in which thermal resistance between heating areas on a surface of the device and a back side of a wiring board is reduced by providing through holes (hereinafter, referred to as "via hole") in a portion of the device, providing plated layers

such as gold plating on a back surface of the device and on side surfaces of the through holes to thereby electrically connect the front and back surfaces of the device via the via holes 5, and using the plated layers as thermal diffusion plates. Generally, the plated layers used as the thermal diffusion plates are called a plated heat sink (PHS) 6.

Meanwhile, a major part of heat generated in circuits formed on the surface of the semiconductor device 1 spreads in a planar-wise manner and passes through the device in a thickness-wise direction, and diffuses in the PHS 6 in a planar-wise manner to be transmitted to the multilayer wiring board. However, a part of such heat gets spreads to locations distant from the heating areas via a wiring layer on the surface of the device to enable reducing thermal resistance to some extent.

In particular, a problem of heat radiation in a planar-wise manner exhibits itself markedly as the semiconductor substrate becomes thin. Conventionally, the above problem has not come to the fore since semiconductor substrates are generally fairly thick enough to be ~~much~~ effective in planar-wise diffusion of heat within a substrate, and distribution of heat flux is substantially uniform on a back surface of the semiconductor substrate. However, ~~when~~ as heating areas in a semiconductor substrate are increased in packaging density and ~~in plan~~ size decreases ~~in plan becomes small~~, thermal

resistance in a thickness-wise direction causes a so much problem, which makes it necessary to make the semiconductor substrate thin and to reduce the thermal resistance.

However, when a semiconductor substrate is made thin, planar-wise diffusion of heat inside of the semiconductor substrate becomes insufficient, and so distribution of heat flux on a back surface of the semiconductor substrate is affected by the calorific value and distribution of heating areas on the front surface of the substrate to lead to an increase of thermal resistance in a planar-wise direction unless heat thermal conductive members such as thermal vias are arranged in appropriate positions. Thus, a problem is caused that thermal resistance is not reduced though the substrate is made thin.

Meanwhile, in designing an arrangement of electrodes and via holes 5 in a plane where circuits of a semiconductor device are formed, it has been conventionally general to align rows of electrodes in position in the case where, as shown in Fig. 11, a plurality of rows of electrodes are connected in parallel to function as one semiconductor element. With such an arrangement, irrespective of whether via holes 5 are arranged in a center or ends of the rows of electrodes, the via holes 5 are arranged substantially in a line in a longitudinal direction in the figure. Moreover, when the number of the electrodes in the

respective rows of electrodes involves no scatter, positions of the electrodes will be also arranged substantially in a line in a longitudinal direction in the figure. However, such an arrangement presents the following issues.

Here, it is assumed that heating areas are mainly constituted by emitter base junctions disposed below emitter electrodes 7. In the case of an arrangement in a cross sectional view shown in Fig. 10, a heating area is in the vicinity of ~~near~~ a junction of a highly doped p type GaAs base layer 18 and a highly doped n type InGaP emitter layer 20. ~~Below an Emitter wiring~~ 10B which is connected to Emitter wiring (noting that the emitter wiring 10B is consisted of a different material from Emitter 10A As described above, heat generated in this area is discharged in a thickness-wise direction of a semiconductor substrate 1 while diffusing in longitudinal and transverse directions in Fig. 11. However, when fingers are laid down as shown in Fig. 11, via holes and ends of rows of electrodes are aligned in position, which causes a problem that fingers arranged in positions distant from the via holes and from the ends of rows of electrodes are restricted in radiation paths to become ~~liable~~ likely to have a significant rise in temperature.

Hereafter, an embodiment of the present invention will be described with reference to Figs. 1 and 2.

Fig. 1 is a cross sectional view showing the positional relationship between a multilayer wiring board according to the present invention and a

semiconductor substrate mounted thereon. In addition, Fig. 1 shows a typical case where a material of the semiconductor substrate 1 is GaAs and circuits are heterojunction bipolar transistors (hereinafter, referred to as "HBT"). However, it goes without saying that a material of the semiconductor substrate 1 is not limited to GaAs, and the circuits are not limited to the HBTs.

Figs. 2A to 2C are views showing, in cross section containing an entire semiconductor substrate, the positional relationship between a multilayer wiring board and a semiconductor substrate. Thus, Fig. 2A is a cross sectional view in an X direction, Fig. 2B is a cross sectional view in a Y direction, and Fig. 2C is a plan view. In addition, while there is no specific limitation on determination of the X and Y directions, it is assumed here that the semiconductor substrate is rectangular in a planar direction and that the X direction is parallel to one side of the rectangle and the Y direction is orthogonal to the X direction.

In Fig. 1, a plurality of emitter electrodes 7 are arranged in rows shown in Fig. 2C, collector electrodes 8 are arranged between the adjacent emitter electrodes 7 in a row, and base electrodes 9 are formed in a manner to sandwich individual emitter electrodes 7 therebetween. It is defined relative to the thickness-wise direction of the semiconductor substrate 1 that a side contacting the PHS 6 is lower, and a side, on

which a circuit surface is formed, is the upper side. At this time, the emitter electrodes 7 and the emitter wirings 10 are shown in the structure shown in Figs. 1 and 2. However, constituent members such as collector wiring, base wiring, other circuit parts, wire pads and so on are omitted for the purpose of simplification.

Emitter electrodes 7 are connected to emitter wirings 10 in Fig. 1 and Fig. 2. In addition, the emitter wirings 10 are connected to the via holes 5 provided in the semiconductor substrate. Side surfaces of the via holes 5 are covered with a material which is the same as that of the PHS 6 and has good thermal and electrical conductivity, or interiors of the via holes 5 are filled with a material which has good thermal and electrical conductivity. In the case where the semiconductor substrate 1 is formed of an electrically conductive material, it is desired that the above-described processing is performed after an insulating film is formed on the surfaces of the via holes 5. Also, the semiconductor substrate 1 is mounted on the multilayer wiring board 3 through a brazing material 2 such as solder and an electrically conductive adhesive. In addition, while the wiring board 3 is multilayered here, the present invention is applicable even to a single-layer wiring board, which has wiring patterns on upper and lower sides thereof.

Thermal vias 4 are arranged on the multilayer wiring board 3. Similarly to the via holes 5, side

surfaces of the thermal vias 4 are formed with a layer of a material, which is thermally and electrically conductive, or interiors of the thermal vias 4 are filled with a material, which is thermally and electrically conductive. In the present invention, an entire area occupied by the via holes 5 is included in an area occupied by the thermal vias 4 in the XY plane in the figure. Therefore, when heat loss generated in emitter base junctions in the vicinity of the emitter electrodes 7 is discharged to a back surface of the multilayer wiring board 3 via the emitter wirings 10 and via holes 5, discharge of heat is effected one-dimensionally in a thickness-wise direction through the via holes 5, brazing material 2, and thermal vias 4 in this order in the semiconductor substrate 1. Accordingly, there is no need for heat transmission in a planar direction in, for example, the PHS layer 6 and the brazing material 2. This it is possible to efficiently discharge heat loss, generated in the emitter base junctions in the vicinity of the emitter electrodes 7, to an underside of the multilayer wiring board 3, and to discharge heat outside of the substrate.

As mentioned above, Figs. 3 and 4 are views showing an exemplary arrangement of a conventional semiconductor substrate 1 and a multilayer wiring board 3, in which the positional relationship between the thermal vias 4 and via holes 5 is not prescribed.

Therefore, there is caused a problem that, as shown in the plan view in Fig. 4, the via holes 5 and thermal vias 4 become out of position relative to each other accordingly, even though the multilayer wiring board 3 has thermal resistance as an element equivalent to that of the embodiment of the present invention shown in Figs. 1 and 2, thermal resistance of the entire structure is increased in terms of radiation paths in the planar direction.

However, in the case where the number of the via holes 5 is plural, as shown in Fig. 2, the number of the thermal vias 4 may also be plural. Even if the number of the thermal vias 4 is one as a whole, or one for each via hole 5, or one for a plurality of via holes 5, the same effect can be achieved in any one of the above cases, so long as that condition is met, in which an entire area occupied by the via holes 5 is included in an area occupied by the thermal vias 4 in the XY plane in the figure. Also, while Fig. 2 shows an arrangement in which the thermal vias 4 are regularly arranged outside the area occupied by the thermal vias 4, the thermal vias 4 are free in cross section, shape, number, and arrangement, provided that the above-mentioned condition is met. So, without other circuit components having large heat loss, it does not matter if any thermal vias 4 are not arranged elsewhere. On the contrary, when there are other circuit components with large calorific values, thermal vias 4 may be separately provided below the circuit

components.

A further embodiment of the present invention will be described with reference to Fig. 5. Fig. 5 is a cross sectional view showing the positional relationship between a multilayer wiring board and a semiconductor substrate mounted thereon in this embodiment. In addition, the same numerals as those in Figs. 1 and 2 designate the same parts or elements as those in the earlier figures, and so an explanation therefor will be omitted.

In this embodiment, an area, in which emitter electrodes 7 is arranged, is included in an area occupied by via holes 4 in a XY plane.

Fig. 6 is a schematic diagram showing radiation paths in a cross section in the embodiment of the present invention shown in Figs. 1 and 2. Heat generated in respective emitter base junctions is mainly divided into a part that goes from the emitter wirings 10 to the underside of the multilayer wiring board 3 via the via holes 5 and thermal vias 4, and a part that directly goes to the underside of the semiconductor substrate 3 not through the emitter wirings 10 while diffusing in the XY directions, and flows in the XY directions in the interior of the multilayer wiring board 3 or in the PHS 6 and the brazing material 2. While heat is finally discharged outside due to heat conduction or heat transmission, thermal resistance of the thermal vias 4 and thermal

resistance of only the multilayer wiring board 3a form a thermally parallel circuit so that a major part of the heat passes through the thermal vias 4 and a minor part of the heat passes through the multilayer wiring board 3 in the thickness-wise direction. The smaller the thermal conductivity of the primary material of the multilayer wiring board 3 is, the larger an amount of heat passing through the thermal vias 4 becomes.

In the embodiment of the present invention shown in Fig. 5, an area, in which the emitter electrodes 7 are arranged, is included in an area occupied by the thermal vias 4 in the XY plane, so that heat going to an underside of the device not through the emitter wirings 10 does not flow in the XY directions, but flows into the thermal vias 4 in a one-dimensional manner. Therefore, it is possible to reduce the total thermal resistance.

A still further embodiment of the present invention is shown in Fig. 7. This embodiment has a feature in that areas, in which via holes 5 and emitter electrodes 7 are arranged, respectively, are included in an area occupied by thermal vias 4 in a XY plane. Therefore, heat loss generated in emitter base junctions in the vicinity of the emitter electrodes 7 comprises a part passing through the emitter wiring 10 and via hole 5 and a part that directly goes to the underside of the semiconductor substrate 1 while diffusing in the XY directions, the both parts flowing

into the thermal vias 4 in a one-dimensional manner, thereby enabling reducing the total thermal resistance from the heating areas to the underside of the multi-layer wiring board 3.

A further embodiment of the present invention is shown in Fig. 8. The embodiment shown in Fig. 8 is substantially the same as that shown in Fig. 5 but is constructed such that thermal vias 4 are not arranged only below emitter electrodes disposed nearest to ends (chip ends in the figure) of the semiconductor substrate 1. When a plurality of emitter electrodes 7 are arranged in rows on the semiconductor substrate 3, with each row having the emitter electrodes connected to the same emitter wiring, temperature of emitter base junctions in the vicinity of the respective emitter electrodes 7 is such that a plurality of emitters are high in temperature for those close to centers of the emitters thus arranged and low in temperature for those in peripheral portions thereof. With a high frequency element such as a power amplifier for portable phones, ~~there is the need of~~ it is necessary to making temperature distribution as uniform as possible because, in particular, when HBTs are mounted, ~~scatter~~ differences in temperature of respective emitters arranged in parallel causes ~~scatter~~ difference in current flowing through the respective emitters, ~~to have~~ creating the possibility that positive feedback is applied to cause oscillation of elements and eventual breakage thereof.

To meet such need, an arrangement is preferable, in which thermal vias 4 are arranged

immediately below those ones of emitters disposed centrally of emitters thus arranged, but not arranged immediately below the emitters in the peripheral portions. As a result, it is possible to preserve thermal resistance of the emitters in the peripheral portions as it is, and to decrease only thermal resistance of ones emitters which are disposed centrally of the emitters thus arranged, so that it is possible to reduce the difference in temperature as well as to reduce the entire thermal resistance.

In addition, the cross sectional views shown in Figs. 1, 5, 7, and 8 depict arrangements in which a single thermal via 4 is allotted to a single via hole 5 and a single thermal via 4 is allotted to six emitter electrodes 7, respectively. However, the thermal vias 4 are free in number, size, and way of arrangement so long as the conditions prescribed in the respective embodiments are met, and so Thus, a single thermal via 4 may be allotted to a plurality of via holes 5 or a one-to-one correspondence may be applied. Also, a single thermal via 4 may be allotted to a plurality of emitter electrodes 7 or a one-to-one correspondence may be applied. Further, Fig. 5 shows an arrangement in which the emitter electrodes 7 are divided into two groups, though there is no showing of any via hole 5. However, it does not matter if the emitter electrodes are divided into a plurality of groups, or arranged individually according to a certain rule.

Also, cross sectional views or plan views

showing the respective embodiments of the present invention shown in Figs. 1, 2, 4, and 7 show arrangements in which only one via hole 5 per row is provided centrally of a row of the emitter electrodes 7 connected to one another by a line of emitter wiring 10. However, the number and arrangement of the via holes 5 are optional for a row of a plurality of emitter electrodes 7 connected to one another by a line of emitter wiring 10, and so it does not matter if one via hole 5 is arranged at both ends of the row and a plurality of via holes are arranged in the row.

Fig. 9 shows a constitution of a further embodiment of the present invention. In this embodiment, emitter fingers 7 are mounted on an SOI (silicon on insulator) substrate 11. With the SOI substrate, individual transistors 12 are enclosed by an insulating film 13 so as to reduce a parasitic capacitance, with the result that the insulating film 13 causes areas occupied by the respective emitter electrodes 7 to be thermally insulated from one another. With such an arrangement, other portions than layers such as emitter wirings 10 cannot serve as a radiation path, so that heat loss generated passes the semiconductor substrate 1 via the emitter wirings 10 and the via holes 5. With such an arrangement, areas occupied by the via holes 5 are made to be included in areas occupied by thermal vias 4 in the XY plane, so that it is still more possible to promote heat

conduction in the thickness-wise direction and to reduce thermal resistance from the heating areas to the underside of the multilayer wiring board 3.

A still further embodiment of the present invention is shown in Fig. 12. Fig. 12 shows the positional relationship among emitter electrodes, emitter wirings, and via holes in this embodiment. In this embodiment, via holes 5 are arranged in positions offset from one another in adjacent rows of emitters. In the case of the arrangement in a conventional semiconductor device shown in Fig. 11, positions of the third and fourth emitter electrodes 7 from the left in the figure and the third and fourth emitter electrodes 7 from the right in the figure are distant from the via holes 5 and also from ends of rows of emitters, ~~thus~~ This causing a problem that adequate radiation paths cannot be ensured and, ~~so~~ accordingly, temperature is liable to rise. However, the arrangement shown in Fig. 12 makes it possible to reduce a distance from an emitter electrode 7 to the via holes 5 which are not arranged in ~~not~~ a row, to which the emitter electrode 7 concerned is connected, but instead to adjacent rows, whereby emitter electrodes 7 having been liable to rise in temperature with a conventional semiconductor device decrease in temperature, ~~making~~ This makes it possible to maintain a constant temperature distribution ~~constant~~ and to reduce thermal resistance of the entire semiconductor device.

A still another embodiment of the present

invention is shown in Fig. 13. Fig. 13 shows the positional relationship among emitter electrodes, emitter wirings, and via holes in this embodiment. Rows of emitters themselves are positionally offset from adjacent rows in this embodiment, and so the via holes 5 are also arranged offset from those in adjacent rows. As a result, heat generated in emitter fingers 7 disposed near ends of rows can be improved in performance of radiation since portions free of heating areas are present in the periphery. Also, heat generated in the emitter fingers 7 distant from ends of rows and also from the via holes 5 in the rows can be improved in performance of radiation of heat discharged to the via holes 5 in the adjacent rows.

In addition, while positions of the via holes 5 and rows of fingers are periodically offset from one another in the embodiment of the present invention shown in Figs. 12 and 13, the present invention has no reason for such periodicity in the way of such offsetting, and so it goes without saying that the same effect can be obtained in that arrangement in which heating areas in the respective emitter fingers are constant in temperature distribution and temperature is decreased as compared with the case where no counter-measure is adopted, though such arrangement deviates somewhat in periodicity.

A further embodiment of the present invention is shown in Fig. 14. Fig. 14 shows the arrangement of

heating areas in the semiconductor substrate 1 and of thermal vias in the multilayer wiring board 3. Thus, this embodiment is obtained by a combination of the embodiment of the present invention shown in Fig. 1 and the embodiment of the present invention shown in Figs. 12 and 13. Such arrangement of heating areas, via holes and thermal vias makes it possible to achieve further reduction of thermal resistance.

In this manner, it is possible according to the present invention to reduce thermal resistance of an entire device, since heat generated in respective heating areas can be effectively conducted to an underside of a multilayer wiring board. Also, since heat generated in respective heating areas can be effectively ~~let out~~ released to via holes and a semiconductor substrate, thermal resistance of an entire device can be reduced.

It is possible according to the present invention to provide a multilayer wiring board having an improved ~~in~~ radiation effect, since radiation paths leading from emitter wirings to an underside of a multilayer wiring board through via holes and thermal vias can be reduced in thermal resistance.